

REMARKS

Reconsideration and allowance of the subject application in view of the foregoing amendments and the following remarks is respectfully requested. Entry of the above amendments under Rule 116 is requested in at least it places this application in condition for allowance.

Claim Status/Amendments

Claims 1 and 4 have been amended to improve syntax and form. These amendments do not change the content of the claims and therefore do not require further consideration/search. Entry of the amendments is therefore seen as being proper at this stage of the prosecution. Claims 1-5 remain pending in the application.

Rejections under 35 USC § 103

Claim 1 is rejected under 35 USC § 103(a) because, according to the Examiner, patent '565 to Kamimura et al discloses all claimed features except the thermal oxidation of the electrodes to form an insulating layer.

Applicants understand from page 8 paragraph 10 of the Office action that the Examiner, in order to reach this conclusion, has chosen not to give any patentable weight to the word "reading" or to the whole recitation of "said electrodes being shift register". It is respectfully submitted that this is not appropriate since the main purpose of the invention, as explained in the specification, is to find a way of building a very small reading diode at the end of a register between a last electrode of the shift register and a reset electrode of the shift register; the purpose of the invention is not to make any contact with any integrated circuit portion using known contacting techniques.

Removing the technical feature of the reading diode and the position of the reading diode amounts to say that the hypothetical person of ordinary skill in the art would give no weight to the purpose of what he is designing, which is not correct. The purpose of the invention is to build a very small reading diode, taking into consideration the location where it must be placed in a shift register.

It is therefore submitted that consideration should be given to these features for determining patentability. Claim 1 has been amended to remove these features from the preamble of the claim and put them at the adequate location in the steps of forming the device, as indirectly suggested by the Examiner in its argumentation paragraph 10.

Amendments to claim 1 comprise only this formal modification as well as the adjunction of a precision regarding the definition of what is a reading diode, i.e. a diode "*adapted for converting into a voltage charges which are conveyed by the shift register*". It is believed that these amendments do not substantially change the definition of the claimed invention because such a definition was already self contained in the wording "reading diode" or "readout diode". A similar amendment has been made in claim 4.

When the above features are considered, it is submitted that the devices and methods disclosed in the cited prior art do not suggest the claimed invention.

a) No reading diode is disclosed in Kamimura. Kamimura discloses a storing diode for producing charges under the influence of light impinging onto the layer above said diode; this storing diode is in no way a reading diode at the end of a shift register. No read function is accomplished by the storing diode of Kamimura. The reading function of the diode at the end of a shift register is very well known in the art: it is a function whereby charges poured into the diode by the shift register are converted into a voltage. The storing diode of Kamimura has no such function. Charges stored in the storing diode of Kamimura are poured into the CCD shift register; there are no charges poured from the shift register into the storing diode. The storing diode in Kamimura should have a maximal size; the reading diode in the invention is designed so as to have a size as minimal as possible.

b) The assertion that Kamimura discloses a diode between a last electrode of the shift register and a reset electrode is incorrect as well (paragraph 4 of the office action). What is disclosed in Kamimura has no relation whatsoever with the construction of the extremity of the shift register, i.e. at the place where a reading diode should be located. Kamimura relates only to the intermediate part of the shift register, where no reading diode can be located as can easily be seen on figure 2 of Kamimura. In addition, there is no reset electrode shown or described in Kamimura.

c) It is assumed that a reading diode would however be present if the hypothetical

person of ordinary skill would build a device according to the method proposed by Kamimura, at the end of the shift register. The reading diode is not visible in Kamimura. The reading diode is not described in Kamimura. The hypothetical person of ordinary skill would build the reading diode as is always done in the art, i.e. typically as disclosed in Fig. 1 of the application under examination, with an aluminum contact between the last electrode and the reset electrode. It is submitted that the hypothetical person of ordinary skill would not locate the reading diode in place of a storing diode in the last register stage, and he would not construct a reading diode in the same way as a storing diode since it has a different function.

d) The Examiner contends that it would have been obvious to form insulating layers on the electrodes by thermally oxidizing the polysilicon layers of the last electrode and reset electrodes of the shift register. However, it is respectfully submitted that the prior art always shows that the contact with a reading diode is made with an aluminum contact, and the aluminum contact precludes having such an insulating layer, unless the aluminum does not contact the thus manufactured insulating layer. Kub '604, although not relating to a reading diode, shows that an aluminum contact is at a distance from the polycrystalline electrode and its insulating layer. Having a construction similar to Kub '604 for building a reading diode would prevent the reading diode from being sufficient small. Stevens shows that the aluminum contact may be in physical contact with the insulating layer because the insulating layer is not thermally grown over the polysilicon layers. Kub '261 shows no aluminum contact because it shows no reading diode.

Rejection of claim 2 based on Zoroglu seems improper since Zoroglu does not mention any nitride deposition, which is a core step of claim 2. The context of the description of Zoroglu would not lead the hypothetical person of ordinary skill to look into Zoroglu to find a method for building a very small reading diode at the end of a shift register.

Similarly, rejection of claim 3 is not understandable since the additional document to Wolf discloses manner of making field oxide as planar as possible during oxidation of the substrate, which does not suggest anything relating to the formation of a polysilicon electrode above a reading diode.

Claim 4 is rejected, based on Stevens anticipating all features of claim 4 except for a number of features. The examiner contends that the hypothetical person of ordinary skill would

have been motivated to add these features in order "to provide interconnect contact for the diode". However, interconnect contact is already present in Stevens and the hypothetical person of ordinary skill would have no motivation for replacing it by something more complicated and not available in standard techniques for making reading diodes. The Examiner contends that one would have been motivated "also because the doped polycrystalline is a functional equivalent of Aluminum". It is submitted that the polycrystalline silicon is not *per se* a functional equivalent of aluminum. In the context of the invention, it is not. One would not understand why Stevens has aluminum layers (45) distinct from polycrystalline layers (16, 20, 22) if polycrystalline silicon would be an equivalent of aluminum. Kub '604' also has both aluminum and polysilicon layers, showing that they are not equivalent. The invention also has aluminum layers distinct from polysilicon layers. Kamimura considers that either aluminum or polysilicon or other materials could be used for contacting a diode, but this does not mean that these materials are all equivalent materials ; they are equivalent only in so far as they would all allow, according to Kamimura, a deposition, over them, of a photoconductive layer according to a specific method claimed in Kamimura. But they are not equivalent in any context.

Claim 5 is rejected further in view of Spangler for the reason that Spangler assumedly disclose nitride layer to cover doped polysilicon to prevent diffusion of impurity. The Examiner notes that the nitride layer would have the same pattern as the polysilicon. This is wrong since, as disclosed in the portion of Spangler cited by the Examiner, the pattern of nitride is defined by an etching step which is independent from the patterning step for polysilicon, which is easy to see on figure 4 of Spangler. In Spangler, layer 160 is a passivation layer, equivalent to layer 18 of the instant application, not equivalent to nitride layer 46 which has a specific role.

In light of the preceding arguments the following rejections are summarily traversed:

1) Claim 1 under 35 USC 103(a) as being unpatentable over Kamimura et al. ('565) and further in view of Kub ('604);

2) Claim 2 under 35 USC 103(a) as being unpatentable over Kamimura et al. ('565) and Kub ('604) and further in view of Zoroglu ('535);

3) Claim 3 under 35 USC 103(a) as being unpatentable over Kamimura et al. ('565), Kub ('604), Zoroglu ('535) and further in view of Wolf (Silicon Processing for the VLSI Era, page 331);

4) Claim 4 under 35 USC 103(a) as being unpatentable over Stevens ('990) and further in view of Kamimura et al. ('565); and

5) Claim 5 is rejected under 35 USC 103(a) as being unpatentable over Stevens ('990), Kamimura et al. ('565) and further in view of Spangler et al. ('064).

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the application is in condition for allowance and a Notice to that effect is earnestly solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,
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